2 Day Workshop on VLSI

Day-1:

Morning session: Introduction to Verilog HDL language.

- Explain the Xilinx vivado tool about front-end explanation.
- Explain the combinational circuits with Verilog and test bench

Afternoon:

- Explain about Inter delay and intra-dealy. Frequency division.
- explain the sequential circuit with the testbench.

Day - 2:

Morning:

- Continue the sequential circuit.
- Explain about the datapath and control path With example.

Afternoon :

- explain about FPGA board and
- Implement and show the demo program on FPGA.

Resource person:Mr.P.Tejeswara Rao

Mr. P. Tejeswara Rao is a dedicated professional with a fervent interest in VLSI and FPGA Prototyping. Currently, he is actively involved in the Research and Development Department focusing on FPGA and VLSI Design at Sense Semiconductors and IT Solutions Pvt. Ltd.